

CLAIMS:

1. A semiconductor processing method, comprising:

providing a silicon nitride material having a surface, the surface comprising a nitrogen barrier region, the nitrogen barrier region comprising silicon and nitrogen;

forming a photoresist over the silicon nitride material surface; and

restricting diffusion of nitrogen from the silicon nitride material to the photoresist with the barrier.

2. The method of claim 1 wherein the barrier comprises silicon oxynitride formed by exposing the silicon nitride material to an atmosphere comprising oxygen.

3. The method of claim 1 wherein the barrier comprises a silicon nitride having a higher concentration of silicon than a remainder of the silicon nitride material.

1 4. A semiconductor processing method, comprising:
2 providing a silicon nitride material having a surface;
3 forming a photoresist over the silicon nitride material surface; and
4 providing a barrier layer between the silicon nitride material and
5 the photoresist, the barrier layer restricting diffusion of nitrogen from the
6 silicon nitride material to the photoresist, and comprising silicon and
7 nitrogen.

8
9 5. The method of claim 4 wherein the barrier layer comprises
10 a thickness of less than or equal to about 5 nanometers.

11
12 6. The method of claim 4 wherein the barrier layer comprises
13 silicon, oxygen and nitrogen.

14
15 7. The method of claim 4 wherein the barrier layer comprises
16 $\text{Si}_x\text{N}_y\text{O}_z$, wherein x, y and z are greater than or equal to 1 and less than
17 or equal to 5.

18
19 8. The method of claim 4 wherein the barrier layer comprises
20 silicon oxynitride formed by exposing the silicon nitride material to an
21 atmosphere comprising oxygen.
22
23

1 9. The method of claim 8 wherein the oxygen is in the form
2 of one or more of ozone, NO or N₂O.

3
4 10. The method of claim 4 wherein the barrier layer comprises
5 silicon oxynitride formed by plasma-enhanced chemical vapor deposition.

6
7 11. The method of claim 4 wherein the barrier layer comprises
8 silicon oxynitride formed by rapid thermal processing.

9
10 12. The method of claim 4 wherein the barrier layer comprises
11 silicon oxynitride formed by high pressure oxidation.

12
13 13. The method of claim 4 wherein the barrier layer comprises
14 silicon oxynitride formed by low pressure oxidation.

15
16 14. The method of claim 4 wherein the barrier layer comprises
17 a silicon nitride layer having a higher stoichiometric amount of silicon
18 than the silicon nitride material.

19
20 15. The method of claim 4 wherein the barrier layer comprises
21 Si_xN_y, wherein x is greater than or equal to y.

1 16. The method of claim 4 wherein the barrier layer comprises
2 a silicon nitride layer having a higher stoichiometric amount of silicon
3 than the silicon nitride material and is formed by chemical vapor
4 deposition in a common and uninterrupted deposition process with the
5 silicon nitride material.

6
7 17. A semiconductor processing method, comprising:
8 providing a silicon nitride material having a surface;
9 forming a barrier layer over the surface of the material, the barrier
10 layer comprising silicon and nitrogen;
11 forming a photoresist over and against the barrier layer;
12 exposing the photoresist to a patterned beam of light to render at
13 least one portion of the photoresist more soluble in a solvent than an
14 other portion, the barrier layer being an antireflective surface that
15 absorbs light passing through the photoresist; and
16 exposing the photoresist to the solvent to remove the at least one
17 portion while leaving the other portion over the barrier layer.

18
19 18. The method of claim 17 wherein the barrier layer comprises
20 a silicon nitride layer having a higher stoichiometric amount of silicon
21 than the silicon nitride material.
22
23

1 19. The method of claim 17 wherein the barrier layer comprises
2 Si_xN_y , wherein x is greater than or equal to y.

3
4 20. The method of claim 17 wherein the silicon nitride material
5 comprises Si_3N_4 , and wherein the barrier layer comprises Si_xN_y , wherein
6 x is greater than or equal to y.

7
8 21. The method of claim 17 wherein the barrier layer comprises
9 a silicon nitride layer having a higher stoichiometric amount of silicon
10 than the silicon nitride material and is formed by chemical vapor
11 deposition in a common and uninterrupted deposition process with the
12 silicon nitride material.

13
14 22. A semiconductor wafer assembly, comprising:
15 a silicon nitride material having a surface;
16 a barrier layer over the surface of the material, the barrier layer
17 comprising silicon and nitrogen; and
18 a photoresist over and against the barrier layer.

19
20 23. The semiconductor wafer assembly of claim 22 wherein the
21 barrier layer comprises a thickness of less than or equal to about 5
22 nanometers.

1 24. The semiconductor wafer assembly of claim 22 wherein the
2 barrier layer comprises silicon, oxygen and nitrogen.

3
4 25. The semiconductor wafer assembly of claim 22 wherein the
5 barrier layer comprises silicon oxynitride.

6
7 26. The semiconductor wafer assembly of claim 22 wherein the
8 barrier layer comprises a silicon nitride layer having a higher
9 stoichiometric amount of silicon than the silicon nitride material.

10
11 27. The semiconductor wafer assembly of claim 22 wherein the
12 barrier layer comprises Si_xN_y , wherein x is greater than or equal to y.

13
14 28. A semiconductor wafer assembly, comprising:
15 a silicon nitride material having a surface and comprising a
16 nitrogen diffusion barrier at the surface, the barrier comprising silicon
17 and nitrogen; and
18 a photoresist over and against the barrier.

19
20 29. The semiconductor wafer assembly of claim 28 wherein the
21 barrier layer comprises a thickness of less than or equal to about 5
22 nanometers.

1 30. The semiconductor wafer assembly of claim 28 wherein the
2 barrier comprises silicon, oxygen and nitrogen.

3
4 31. The semiconductor wafer assembly of claim 28 wherein the
5 barrier comprises silicon oxynitride.

6
7 32. The semiconductor wafer assembly of claim 28 wherein the
8 barrier comprises Si_xN_y and a remainder of the silicon nitride material
9 comprises Si_sN_t , a ratio of x to y being greater than a ratio of s to t.

10
11 33. The semiconductor wafer assembly of claim 28 wherein the
12 barrier comprises a greater concentration of silicon than a remainder of
13 the silicon nitride material.